Doped Conjugated Polymer with Memory Effects and Synapse Transistor Behaviors

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【ABSTRACT】

Artificial synaptic transistor with both the low energy consumer and highly parallel operation advantages which has been received great attention recently. In this study we exploit a simple and effective strategy for fabrications of transistor-type nonvolatile memory device with synaptic behaviors. The synaptic behaviors are induced by an ionic dopant without using any extra charge-storage layer. After doping the memory window has significant increase the memory window of approximately 70% with an on/off current ratio over 10^3. Moreover, the doped device successfully mimics synaptic functions like excitatory post synapse current, pair-pulse facilitation, and spike timing depend plasticity. The paired-pulse facilitation index over 200% has been achieved. The doped device possesses learning availability and memory characteristics. In this work, we not only verify the doped device with enhanced memory property but also manifests the synaptic transistors without using any charge storage layer possible.

【INTRODUCTION】

Inspired by human neural system, the brains are composed of billions of neurons and can perform complex processing and storage capability. By contrast, the traditional computers with separated memory modules and processors result in high energy consumption and limited parallel computation, so called von Neumann bottleneck. Hence, it is important to develop electronic components to mimic the neuron behaviors to improve energy consumption and data process efficiency. Recently, several synapse devices have been reported, e.g., two terminal memristors[1], phase-change memory, and three-terminal transistor-type memories. Three-terminal transistors have been considered as an ideal device structure for synaptic device[2]. Three-terminal transistor memories[3], or called synaptic transistors, contain many advantages, including the ability to mimic synapse behavior, lower power consumption, and easy integration with circuits. This features reveal promising potential for neuromorphic electronics.

A synaptic transistor consists of transistor and memory characteristics. Hence it is able to mimic the neuron with processes computation and storage function. To realize the bi-functional single device, researchers commonly require complex device structure, e.g., floating gate, to control the drain-source current. However, this structure easily results in unintentional increases

of fabrication cost and current leakage risk.

In this work, we propose a p-type D-A conjugated polymer doped with ionic salt to control current hysteresis and charge storage capability without using floating gates. The doping effect not only enhances the trapping charge ability but also performs many synaptic characteristics. The memory and synaptic behaviors are demonstrated.

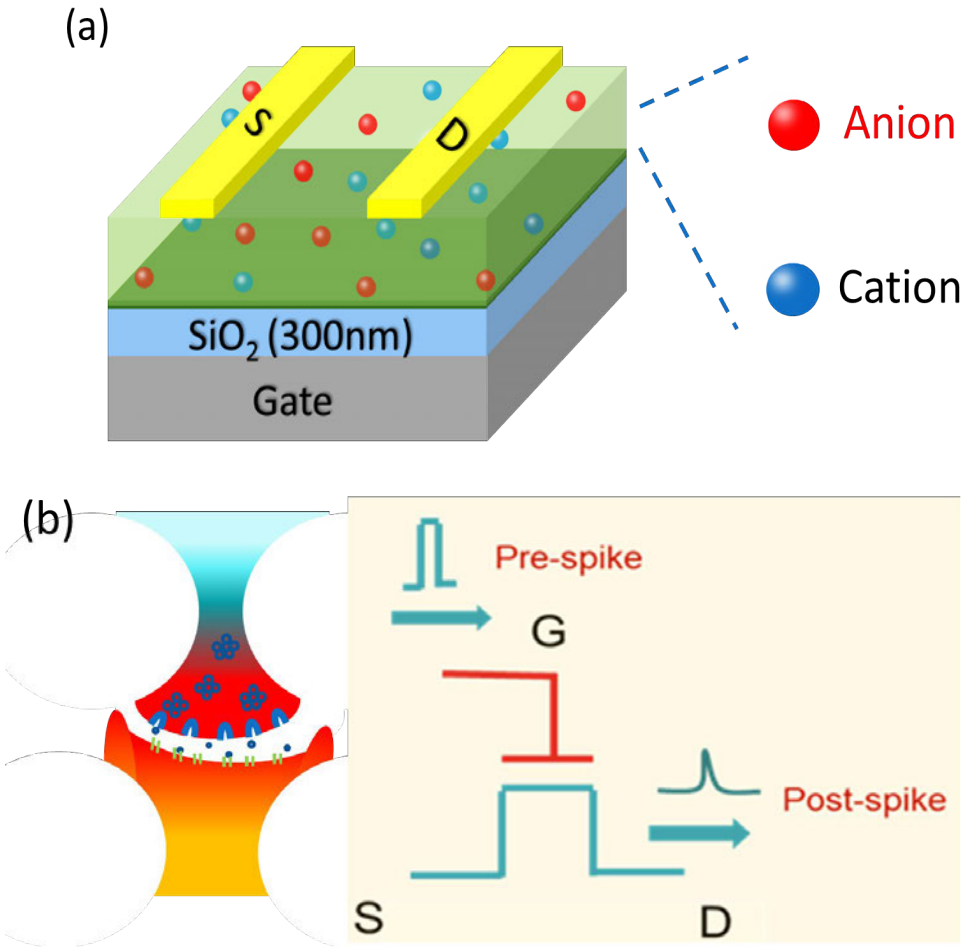

Figure 1. (a) The device structure of the ion-doped synaptic transistors and (b) schematic synaptic behaviors mimicked by the synaptic transistors.

【EXPERIMENT】

A bottom-gate/top-contact structure was employed for the fabrications of transistor-type memories. A silicon wafer with a 300-nm-thick SiO2 dielectric layer (C_i = 10 nF cm-2) was used as the substrate. These wafers were first cleaned by oxygen plasma for 5 minutes at a power of 120 W under an oxygen pressure of 300 torr. Sequentially, the wafers were modified with OTS self-assembly monolayer (SAM). After modifying with OTS SAM on the surface of SiO_2/Si substrates, the surface showed the contact angle of 108°. The doped polymer layers were spin-coated onto the OTS-treated SiO_2/Si substrates at a spin rate of 3000 rpm for 60 s, followed by annealing at 150 °C for 1 hr in the N2-filled glove box. The polymer solutions were prepared in chlorobenzene with a concentration of 5 mg mL^{-1}. The solution was preheated at

90°C overnight to improve solubility in the organic solvent. Finally, a 80-nm-thick gold electrode was defined through a shadow mask, where the channel length (L) and channel width (W) are 50 μm and 1000 μm, respectively. The transfer and memory characteristics are measured in a N2-filled glove box by using Keithley 2634B semiconductor parametric analyzer.

【RESULTS & DISCUSSION】

Figure 2a presents the typical transfer curves under a dual sweeping mode of the transistor-type memory devices based on the doped polymers with various doping ratio from 0% to 10%. As seen in the transfer curves, the current hysteresis increases with the increased ionic dopant ratios. The reason for the increased current hysteresis may be attributed to the formation of the charge trapping site induced by the dopant. This leads to enhancing electron charge trapping and the memory behaviors. Furthermore, the charges on the organic salt may transfer to the conjugated polymer, leading to doping effects. These characteristics show that the ionic dopant has the great potential for the applications of the synaptic transistors.

To evaluate the performance of the synapse transistor, we first investigate the current response of the devices under the continuous pulse stimuli, as present in **Figure 2b**. The current response under the continuous pulse stimuli is referred as excitatory post-synapse current(EPSC). The second peak showed the enhancement of the current respons. This is attributed to the fact that the first pulse causes the formation of the charge residual in the channel. Thereby, the second pulse can be enhanced owing to the charge residuals induced by the first pulse in millisecond**.** From the current increase, we can estimate a paired-pulse facilitation index (PPF). The PPF value is over 200 % when giving fast pulse stimuli. **Figure 2c** exhibits the EPSCs induced by presynaptic spikes with various time intervals from 10 to 500 ms. As seen in Figure 2c, the short time interval gives higher current response. The PPF index increases, when the pulse interval is small**.**

【CONCLUSION】

In this work, we demonstrate a facile method to fabricate synaptic transistors. After doping ion dopant, the current response is significantly improved. More importantly, the transistor-type device manifests the high pair-pulse facilitation(PPF) index and¥ mimic the others synaptic function like excitatory post synapse current (EPSC). In this study, we demonstrate the facile method to fabricated the transistor memory device with synaptic transistors.

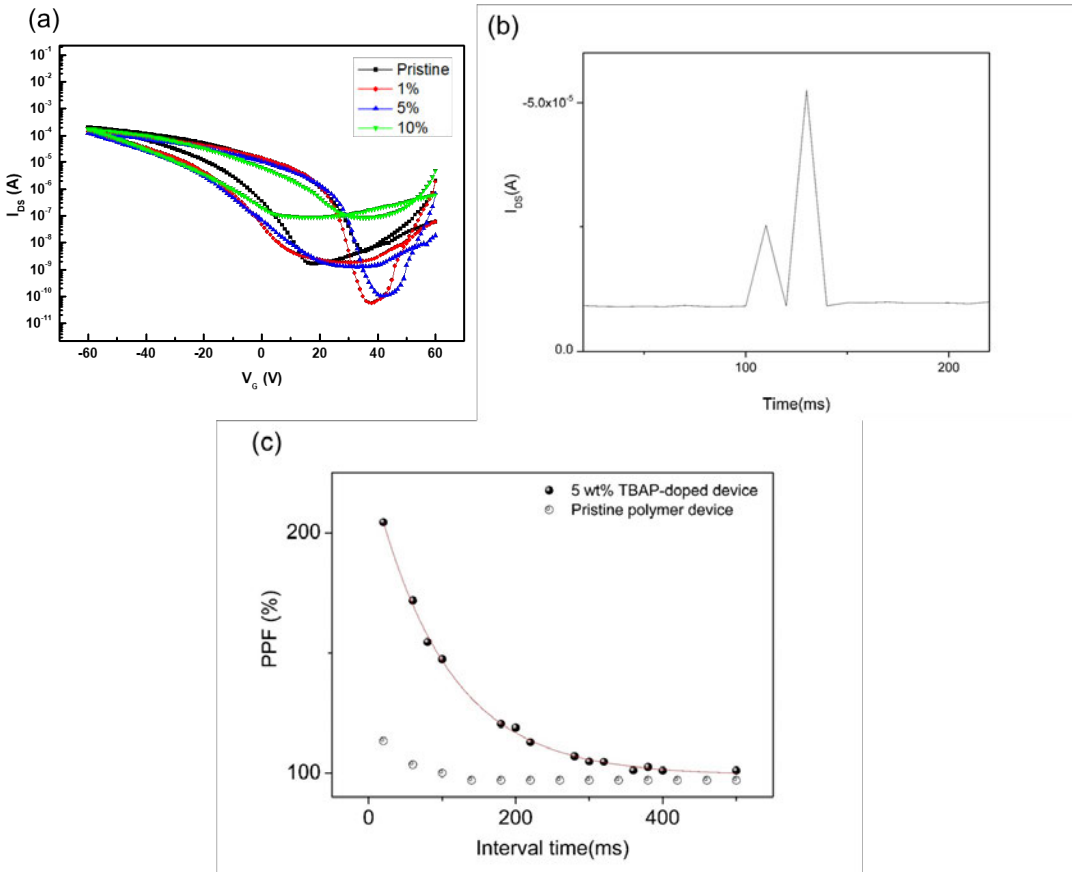

Figure 2. (a) dual swept transfer curves of the doped polymer devices. (b) The EPSC of the polymer film; (c) The relationship between PPF and interval times for the synaptic transitors.

【REFERENCES】

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